Intel® Xeon™ Processor with 512 KB L2 Cache Signal Integrity Model Usage Guidelines, Revision 2.01

February 2002

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1. Revision History

Revision	Description	Date
2.0	Initial release.	January 2002
2.01	Added length adjustment worksheet for platforms based on the Intel Xeon processor with 512 KB L2 cache with the Intel® E7500 chipset. Minor updates and corrections to model_usage_guide.pdf document.	February 2002

2. Customer Support

For model support, please contact your Intel field representative. For usage or conversion support contact your simulation tool vendor representative.

3. Release Contents

Enclosed are revision 2.0 signal integrity models for the Intel® Xeon™ processor with 512 KB L2 cache. These models are based on completed simulation and validation of the processor I/O buffer design and package.

IBIS Checker:
The version 3.2.7 IBIS checker was used to test the format and syntax of the .ibs model files. No warnings were generated for the cpu_mid_model1.ibs, cpu_mid_model5.ibs, and cpu_mid_model6.ibs files. 2 warnings were generated for the cpu_mid_model2.ibs, cpu_end_model1.ibs, cpu_end_model2.ibs, cpu_end_model5.ibs, and cpu_end_model6.ibs files. These warnings are documented in ibis_checker.log and pertain to slight differences between the endpoint of the I-V data compared to the endpoint expected by the checker. These differences were evaluated to have negligible effect on model accuracy and performance.

File	Description
cpu_end_model1.ibs cpu_end_model2.ibs cpu_end_model5.ibs cpu_end_model6.ibs	Processor I/O buffer models for data, address, and common clock signals in IBIS 3.1 format for the end agent processor.
cpu_mid_model1.ibs cpu_mid_model2.ibs cpu_mid_model5.ibs cpu_mid_model6.ibs	Processor I/O buffer models for data, address, and common clock signals in IBIS 3.1 format for the middle agent processor.
cpu_misc.ibs	Processor I/O buffer models for asynchronous GTL+, TAP, and BCLK receiver sgnals in IBIS 3.1 format.
ibis_checker.log	Log file from the IBIS checker (IBIS Version V3.2.7)
model_usage_guide.pdf	This document.
*.rlc files	Package files in H-Spice format.
package.tlp	Sample processor package files.
E7500_Length_Adj_R2_0.xls	To be used for design of Intel Xeon processor with 512 KB L2 cache/Intel E7500 chipset-based system bus designs.

..\checker\checker_usage_guide.pdf	Usage document for overshoot/undershoot checker utility.
..\checker\gowsim_nt.exe ..\checker\gowsim_hp ..\checker\gowsim_ibm ..\checker\gowsim_linux ..\checker\gowsim_sun	Overshoot/undershoot checker utilities.

4. Introduction

This document describes the models and simulation methods to verify the Intel® Xeon™ processor with 512 KB L2 cache meets signal integrity and timing requirements at the supported data transfer rate of 400M/Ts in dual processor platforms. The intent is to enable the user to create simulation runs that stress timing and noise margins to verify adherence to the specifications documented in the *Intel® Xeon™ Processor with 512 KB L2 Cache* Datasheet.

To simulate signal integrity effects such as ringback or overshoot/undershoot, certain combinations of pull-up and pull-down strengths, edge rate, IO pad capacitance, and package characteristics must be present. The driver and package models that define the worst-case corner behaviors are detailed in this document.

Package models are supplied individually and matched with the appropriate driver in simulation to create the necessary corner conditions. The package models represent the high, nominal, and low impedance geometry, and the maximum cross talk condition.

For dual-processor platforms based on the Intel Xeon processor with 512 KB L2 cache with the Intel® 860 chipset, the Length Adjustment Worksheet provided with the *Intel® Xeon™ Processor I/O Buffer Models* available on http://developer.intel.com should be used. For dual-processor platforms based on the Intel Xeon processor with 512 KB L2 cache with the Intel® E7500 chipset or Intel® E7500 chipset, the length-matching spreadsheet included in this release should be used.

5. Design Space Exploration

To understand the sensitivity and stability of a system under design, Monte Carlo simulation methods are employed. Data analysis focuses on determining the input parameter to output correlation for system variables. The sensitivity of each system variable is assessed and values necessary for creating corner conditions determined.

In the Monte Carlo simulation, all systematic parameters are varied randomly within their tolerance ranges. Variables such as dielectric constant, trace impedance, socket parasitic, and trace line length tolerances are included in the Monte Carlo simulation runs. Initial system characterization runs of approximately 1000 permutations may be sufficient. By running Monte Carlo simulations during the initial design phase, the designer will gain an understanding of the relationships between system variables and system performance.

Table 1 describes the driver/package models recommended for these Monte Carlo simulation runs. The end and middle agent drivers are named CPU_END_MODELx and CPU_MID_MODELx respectively, where ‘x’ is replaced with the correct model number shown in the tables.

Monte Carlo				
Simulation corner	End agent driver	Middle agent driver	Package model	Package length
Full randomized parameter sweep	1, 2, 5	1, 2, 5	Nominal	Nominal

Table 1: Monte Carlo Sweep Analysis.

Table 2 identifies the worst-case simulation corners for system stability to be verified with driver/package/trace model combinations.

Worst Case System Corners	
Corner	Condition
1	Overshoot
2	Undershoot
3	High Side Ring Back
4	Low Side Ring Back
5	Max T-flight
6	Min T-flight

Table 2: Worst Case System Corners

Once system corners and parameter significant lists have been identified, it is recommended that systematic parameter sweep simulations be run with each of the driver/package/trace model significant list combinations. This will allow the designer to define specific simulation corner conditions and parameters for tolerance analysis. The worst-case corners were determined for the layout guidelines documented in the *Intel® Xeon™ Processor and Intel® 860 Chipset Platform Design Guide*.

6. Socket, Interposer, & Package Modeling

The 603-pin socket modeled with discrete inductors, capacitors and resistors is shown in Figure 1.

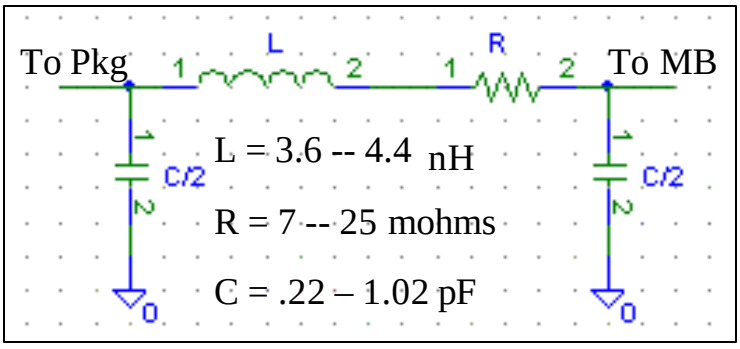

Figure 1: Socket Model

This socket model is currently implemented as a lumped element model. The model is representative of nominal socket electrical parameters. No corner model conditions of high/low impedance were assumed given limited correlation data of possible impedance shift at the time the model was developed.

The Intel Xeon processor with 512 KB L2 cache FC-BGA2 package sits on an interposer, which holds the signal and power supply pins.

- The interposer is modeled as symmetric stripline traces.
- Interposer trace width is nominally 3.5 mils.
- Interposer trace impedance should be simulated from 45 to 55 ohms.
- The trace lengths on the interposer, including the vias, are all 90 mils.

The package I/O model consists of a transmission line segment that represents traces routed in an FC-BGA2 package. The segment consists of the die bump parasitic, package trace, plated through-hole (PTH) via parasitic, and package land parasitic. These components are displayed in Figure 2. In addition, each segment #2 package trace consists of 3 coupled transmission line traces and includes both DC and frequency dependent losses (skin effect). The L's and C's were generated at 200 MHz by solving 2D models. The 2D models were constructed from Induct and Innoveda* XFX*. The Highest and Lowest Zo models are provided to address performance metrics. The models provided for each metric were skewed statistically to their corresponding 4-sigma values. The matrices for all of the models are distributed transmission line parameters and are provided in Quad* XNS* .tlp file format.

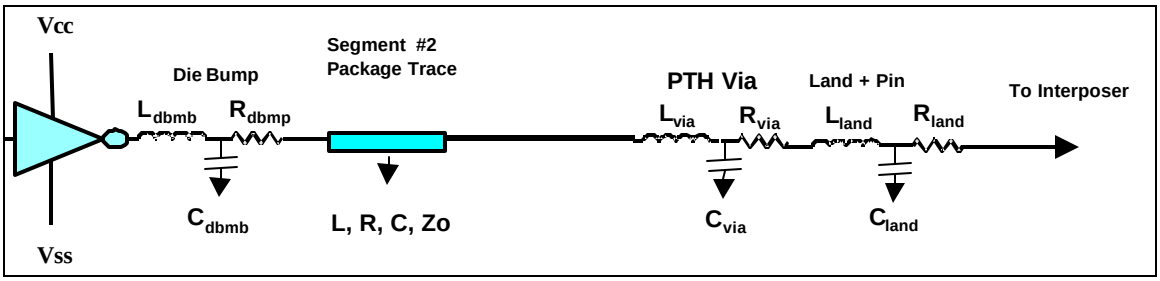

Figure 2: Generic Processor Package I/O Model.

Package Model Limitations/Assumptions:

1) This model assumes ideal ground planes for the Vss planes.
2) Package models assume symmetric stripline throughout.
3) Manufacturing tolerances apply to transmission line segments only
4) L and C were extracted at 200 MHz

In conjunction with the package transmission line parameter files, the exact Segment #2 package trace line lengths for each data\address signal and strobe signals should be used. These package lengths are contained in the the Intel E7500 chipset length-matching spreadsheet:

Model Type	L_{dbmp} pH	R_{dbmp} m?	L_{via} pH	R_{via} m?	L_{land} pH	R_{land} m?	C_{dmp} pf	C_{via} pf	C_{land} pf	Zo ohm	Er
Low Zo	20	2	470	2.1	128	6	0.2	0.03	0.05	46 +/- 12%	3.5 +/- 10%
High Zo	20	2	570	2.1	168	6	0.2	0.03	0.05	46 +/- 12%	3.5 +/- 10%

Table 3: Processor Package Model Characteristics.

7. Test Load Correction

System flight times must be corrected to eliminate double counting of the driver rise/fall time, and to correct device timings for system loading effects. It is necessary to subtract the rise/fall delay of the buffer driving into a standard test load from the driver-to-receiver propagation delay in the system.

For each simulation run, the correction factor corresponding to the active driver should be subtracted from the measured flight time. Proper use of the correction factor requires that simulation time zero begin at the moment of voltage change at the driver pad. If this is not the case, the user should define a correction factor based on the standard load provided.

Figure 3 identifies the standard test load for flight time correction. The flight time correction is measured at the pad of the driver driving into the standard test load, and timing measured from voltage change to the voltage reference level, Vref. Flight time correction and correlation of the driver model to transistor level models can be measured by driving into the standard test load. Processor driver models have been driven into the standard tester load. Table 4 documents the measured flight time correction factors done using Innoveda* XTK for the processor and they correlate well with SPICE transistor level simulations into the test load. Table 4 documents the measured flight time correction factors done using QUAD for the processor and they correlate well with SPICE transistor level simulations into the test load The results of individual signal integrity simulation tools may vary and the user is responsible to determine the correction factors for his own simulation tool.

Model	Time to VM [ns]			
	Rising (at pad)		Falling (at pad)	
	Min [Vref - 10%Vref]	Max [Vref +10%Vref]	Min [Vref +10%Vref]	Max [Vref - 10%Vref]
1-End	0.27	0.34	0.28	0.33
2-End	0.47	0.62	0.70	0.79
5-End	0.27	0.33	0.31	0.36
6-End	0.43	0.52	0.65	0.72
1-Middle	0.23	0.27	0.24	0.29
2-Middle	0.39	0.48	0.63	0.74
5-Middle	0.22	0.26	0.27	0.32
6-Middle	0.35	0.43	0.58	0.67

Table 4: Measured Flight Time Correction Factors.

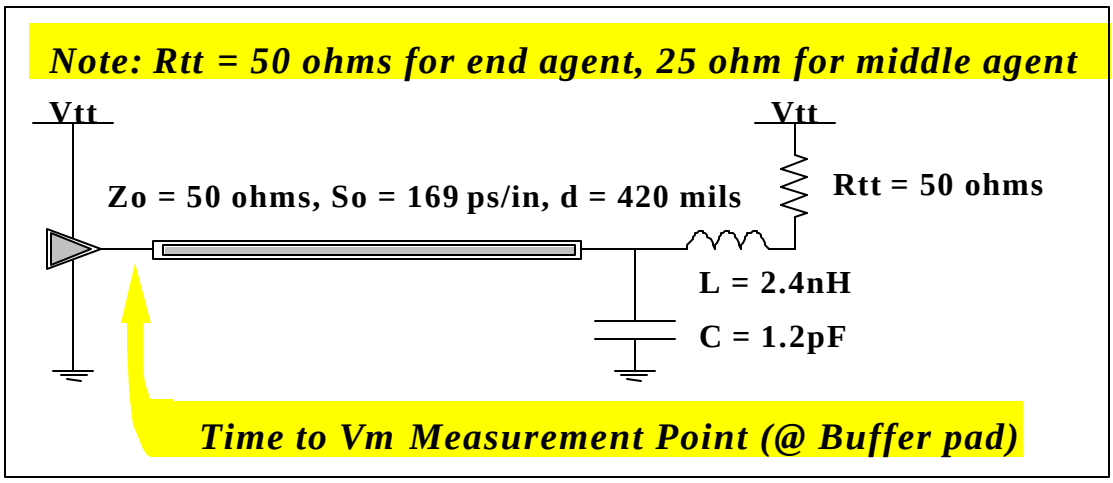

Figure 3: Standard Test Load

8. Simulation and Model Usage

By running Monte Carlo simulations during the initial design phase, an understanding of the relationships between system variables and system performance is used to define the worst case corners. Sensitivity of each system variable was assessed and values necessary for creating corner conditions determined. For each of the case simulation corners, a combination of drivers, package, and system board interconnect parameters was defined among the agents in the system.

9. Processor Corner Conditions

The corner conditions to verify voltage and timing for the processor are detailed in this section. The requirements include common clock, signal quality, and source synchronous signaling conditions be met under allowable spec ranges.

Common Clock

Table 5 identifies the I/O buffer models and topology; exercised to verify processor system bus timing and voltage specs meet allowable budgets and layout guideline requirements, under common clock conditions.

Common Clock Flight Time Corners				
Simulation corner	End agent driver	Middle agent driver	Package model	Package length
Minimum rise time	2	2	Low Z	Short
Maximum rise time	5	5	High Z	Long
Minimum fall time	2	2	Low Z	Short
Maximum fall time	5	5	High Z	Long

Table 5: Processor I/O model usage for common clock simulations

Signal Quality

Table 6 identifies the I/O buffer models and topology; exercised to verify processor system bus timing and voltage specs meet allowable budgets and layout guideline requirements, under common clock conditions for the processor.

Common Clock Signal Integrity Corners				
Simulation corner	End agent driver	Middle agent driver	Package model	Package length
Overshoot	1	1	Low Z	Short
Undershoot	1	1	Low Z	Short
High side Ringback	2	2	High Z	Long
Low side Ringback	2	2	High Z	Long

Table 6: Processor I/O model Usage for Signal Quality Simulations

Source Synchronous

Source synchronous bus operation depends on electrical similarity between data and strobe signal paths. Deviations of board impedance, driver/receiver pad capacitance, and etc. cause setup and hold margin at the receiver to be eroded from the Tvb/Tva present at the driver. Flight time skew simulations should be run to find the worst-case timing difference between data and strobe signals in a single system.

The electrical differences between data and strobe signals within a single system must be characterized in order to set up flight time skew simulations correctly. Monte Carlo simulation will help the designer to find the conditions that create the slowest and fastest system behavior (see section “Design Space Exploration”).

To simulate source synchronous flight time skew, the correct combinations of simulations must be run. There are two basic timing conditions that must be analyzed:

Setup Skew: Data arrives late relative to the associated strobe signal. Data simulation is slow, strobe simulation is slow shifted. Skew, in this case, is measured as the maximum data flight time minus the minimum strobe flight time[1].

Hold Skew: Data arrives early relative to the associated strobe signal. Data simulation is fast, strobe simulation is fast shifted. Skew, in this case, is measured as the minimum data flight time minus the maximum strobe flight time.

Table 7 identifies the I/O buffer models and topology; exercised to verify system bus timing and voltage specs meet allowable budgets and layout guideline requirements under source synchronous conditions for Intel Xeon processor with 512 KB L2 cache-based systems. Similarly,
Table 7 identifies the I/O buffer models and topology; exercised to verify system bus timing and voltage specs meet allowable budgets and layout guideline requirements under source synchronous conditions for Intel® Xeon™ processor with 512 KB L2 cache-based systems.

Source synchronous Flight Time Corners				
Simulation corner	End agent driver	Middle agent driver	Package model	Package length
Setup Skew	2	2	Low Z	Short
Setup Skew	5	5	High Z	Long
Hold Skew	2	2	Low Z	Short
Hold Skew	5	5	High Z	Long

Table 7: Processor I/O model usage for source synchronous simulations[1]

Signal Quality

Table 8 identifies the I/O buffer models and topology; exercised to verify system bus timing and voltage specs meet allowable budgets and layout guideline requirements under source synchronous conditions for the processor.

[1] In all cases, strobe flight times are measured on the signal's falling edge.

Source Synchronous Signal Integrity Corners				
Simulation corner	End agent driver	Middle agent driver	Package model	Package length
Overshoot	1	1	Low Z	Short
Undershoot	1	1	Low Z	Short
High side Ringback	2	2	High Z	Long
Low side Ringback	2	2	High Z	Long

Table 8: Processor I/O Model Usage for Signal Quality Simulations

10. Appendix

Model Characterization for Intel® Xeon™ Processor with 512 KB L2 Cache:

Model	Temp [C]	Process	Vtt [V]	Ron [ohm]	Rtt/P-kicker [ohm]
1-End	100	Fast	1.5	10.03	47.8
2-End	0	Typical	1.5	10.01	50.6
5-End	100	Fast	1.30	10.05	52.7
6-End	0	Typical	1.30	9.38	48.3
1-Middle	100	Fast	1.5	10.03	20.1
2-Middle	0	Typical	1.5	10.01	18.01
5-Middle	100	Fast	1.30	10.05	28.6
6-Middle	0	Typical	1.30	9.38	22.5

11. Customer Support

For usage or conversion support contact your simulation tool vendor representative.